Amendments to the Specification

At page 1, line 9 through line 19, please delete the current paragraph and replace it with the following paragraph:

Fig. 1 shows a typical situation that requires synchronization of an asynchronous data signal. In this example, a memory controller 10 generates a clock signal 12 that is in turn provided to a memory device 14 to coordinate data transfers. In response to clock signal 12, memory ~~component~~ device 14 generates a data signal 16 that is in turn received by the memory controller 10. Although the data signal is generated synchronously with clock signal 12, propagation delays between the memory device 14 and memory controller 10 cause the data signal to lose synchronization by the time it reaches controller 10. Furthermore, propagation delays are different for the different memory devices of the system, so that received data signals will have different phases depending on their sources. This brings about the need for synchronization within controller 10.

At page 2, line 22 through page 3, line 5, please delete the current paragraph and replace it with the following paragraph:

To ensure adequate setup and hold times at the input of latch 26, latches 26a and 26b are configured to clock CDATA either in phase with CLK2 or at 180° relative to CLK2, depending on the phase relationship of CLK2 to CLK1. Specifically, each of latches 26a and 26b receives CDATA as a data input. Latch 26a is clocked by CLK2 and Latch 26b is clocked by CLK2* (the "*" symbol is used to indicate negation or inversion). The outputs of the latches 26a and 26b are connected to the inputs of a two-to-one multiplexer 27. Depending on the value of its select input, the multiplexer presents either the clocked signal from 26a or the clocked signal from latch 26b.

At page 8, line 24 through page 9, line 5, please delete the current paragraph and replace it with the following paragraph:

Phase detection logic 60 generates a detect signal 62 to indicate the result of comparing PHASE1 to the reference value. Circuit 40 includes latching logic 64 that is responsive to phase detection logic 60 and detect signal 62 to latch captured data signal CDATA at an appropriate time or phase relative to CLK2. ~~Latching logic 62~~ Latching logic 64 in this embodiment comprises latch 48 in combination with a two-to-one multiplexer 66. Depending on whether detect signal 62 is true or false, multiplexer 66 supplies CLK2 or CLK2* to the clock input of latch 48.